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10/721,437	11/24/2003	Walter Anthony Wohlmuth	TRQ-00004	7134

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
11/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/721,437	WOHLMUTH, WALTER ANTHONY	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 28-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *0907*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 08/27/2007.

Claims 1-17 and 28-33 are active in this application.

Claim(s) 18-27 have been cancelled.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 09/07/2007. The references cited on the PTOL 1449 form have been considered.

Remarks

3. Applicant's arguments, filed 08/27/2007, have been fully considered. Applicant's Representative, Mr. Joseph A. Pugh, is thanked for the telephonic response on 11/10/2007 relating to an attempt to amend the claim to put it in condition for allowance. Particularly, an attempt to change the word "coupled to", through out the claim, to – in contact with – had been tried; however, even upon such change, the claim would still not be allowable for the reasons given below. Applicant's arguments are also moot in view of new ground of rejection to Imoto et al. (US 6,166,404).

Claim Objections

4. Claim 12 is objected to because of the following reasons: in claim 12, line 6-7, in the phrase "a single etch stop layer overlaid by at least by a first layer", later "by" (line 7) should be deleted to put the claim in better form. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,078,067 to Oikawa.

Regarding claim 1, Oikawa discloses an integrated circuit, as shown in figs. 3-5, comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure,

wherein the multi-layer structure includes a semiconductor substrate 301 overlaid with a plurality of epitaxial semiconductor layers 302-309 common to the D-mode and E-mode FETs, including a channel layer 303 overlaid by a single barrier layer 304 (not that layer 304 of Oikawa is not an etch stop layer stated by Applicant in the Remarks, page 10) as overlaid by a single etch stop layer 308 overlaid by a first layer 309,

wherein the D-mode and E-mode FETs each include source/drain contacts 317-320, and a gate contact 315/316, and

wherein the respective source and drain contacts 317-320 of the D-mode FET and E-mode FET are coupled to the first layer 309, and the respective gate contacts 315/316 of the D-mode FET and E-mode FET are coupled to the single barrier layer 304 (note that all of the layers in the structure are physically and electrically coupled to each other, either directly or indirectly. For example, gate 315 is directly, physically and electrically, coupled to barrier layer 304, while gate 316 is indirectly coupled to barrier layer 304; that is, gate 316 is coupled to barrier layer 304 via layers 307, 308).

Regarding claim 28, Oikawa discloses an integrated circuit, as shown in figs. 3-5, comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure 301-310,

wherein the multi-layer structure includes a semiconductor substrate 301 overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETs, including a channel layer 303 overlaid by a single barrier layer 304 overlaid by a single etch stop layer 308 overlaid by a first layer 309,

wherein the D-mode and E-mode FETs each include source/drain contacts 317-320, and a gate contact 315/316, and

wherein the respective source and drain contacts 317-320 of the D-mode FET and E-mode FET are coupled to the first layer 309, the gate contact 315 of the E-mode FET is coupled to, or in direct contact with, the single barrier layer 304, and the gate contact 316 of the D-mode FET is coupled to, or in direct contact with, the single etch stop layer 308.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim(s) 2-17, and 29-33 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,078,067 to Oikawa., as applied to claim 1 above, and further in view of U.S. Patent No. 6,452,221 to Lai et al.

Regarding claim 2, Oikawa discloses the integrated circuit comprising all claimed limitations, as discussed above, except for further comprising a solid state amorphization region beneath the E-mode gate contact at least within the barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Oikawa to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 3, Oikawa/Lai discloses the integrated circuit wherein the solid state amorphization region includes at least one compound including at least one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 4, Oikawa/Lai discloses the integrated circuit wherein the solid state amorphization region includes a plurality of compounds, wherein at least one of the compounds includes one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium, and at least one of the compounds includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 5, Oikawa/Lai discloses the integrated circuit wherein the multi-layer structure further comprises at least an epitaxial second layer 307 between the barrier layer 304 and the first layer 309. See figs. 3-5 of Oikawa.

Regarding claim 6, Oikawa/Lai discloses the integrated circuit wherein the barrier layer 304 is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the solid state amorphization region is within the implant region. See figs. 3-5 of Oikawa and fig. 1, and col. 2, lines 55-65 of Lai.

Regarding claim 7, Oikawa discloses an integrated circuit, as shown in figs. 3-5, comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure 301-310,

wherein the multi-layer structure 301-310 includes a semiconductor substrate 301 overlaid with a plurality of epitaxial semiconductor layers 302-310 common to the D-mode and E-mode FETs, including a channel layer 303 overlaid by a single barrier layer 304 overlaid by a single etch stop layer 308 overlaid by a first layer 309 overlaid by a second layer 310 adjacent to the first layer 309,

wherein the D-mode and E-mode FETs each include source/drain contacts 317-320, and a gate contact 315/316,

wherein the source and drain contacts 317-320 of the D-mode FET and the E-mode FET are coupled to, or in direct contact with, the second layer 310 (physically),

wherein the gate contact 316 of the D-mode FET is indirectly coupled to the first layer 309 (via layers 321), and

wherein the gate contact 315 of the E-mode FET is coupled to, or in direct contact with, the single barrier layer 304.

Oikawa does not teach a solid state amorphization region beneath the D-mode gate contact within the first layer and a solid state amorphization region beneath the E-mode gate contact within single the barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Oikawa to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 8, Oikawa/Lai discloses the integrated circuit wherein the etch stop layer 308 has a different composition than the first layer 309 and the barrier layer 304, and wherein the D-mode solid state amorphization region is within the etch layer. See col. 2, line 62 col. 4, line 59 of Oikawa, and col. 3, lines 18-27 of Lai.

Regarding claim 9, Oikawa/Lai discloses the integrated circuit comprising all claimed limitations. See col. 2, line 62 col. 4, line 59 of Oikawa, and col. 3, lines 18-27 of Lai.

Regarding claim 10, Oikawa/Lai discloses the integrated circuit wherein the D-mode and E-mode solid state amorphization regions include at least one compound

including platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 11, Oikawa/Lai discloses the integrated circuit comprising all claimed limitations. See col. 3, lines 18-27 of Lai.

Regarding claim 12, Oikawa discloses an integrated circuit, as shown in figs. 3-5, comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure,

wherein the multi-layer structure includes a semiconductor substrate 301 overlaid with a plurality of epitaxial semiconductor layers 302-309 common to the D-mode and E-mode FETs, including a channel layer 303 overlaid by a single barrier layer 304 overlaid by a single etch stop layer 308 overlaid by at least by a first layer 309;

wherein the D-mode and E-mode FETs each include source/drain contacts 317-320, and a gate contact 315/316,

wherein the source and drain contacts 317-320 of the D-mode FET and the E-mode FET are coupled to, or in direct contact with, layer 309 overlying the channel layer 303,

wherein a gate contact 316 of the D-mode FET is coupled to one of the first layer and the single barrier layer 304 (the gate contact 316 is indirectly physically coupled to the first layer 309 as well as indirectly physically/electrically coupled to the barrier layer 304),

wherein a gate contact 315 of the E-mode FET is indirectly physically coupled to the first layer 309 as well as directly coupled to, or in contact with, the single barrier layer 304.

Oikawa does not expressly teach about a solid state amorphization region beneath the E-mode gate contact at least within the single barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the E-mode gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Oikawa to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 13, Oikawa/Lai discloses the integrated circuit wherein the D-mode gate contact 316 is coupled to the first layer 309 (physically), and the E-mode gate contact 315 is coupled to the barrier layer 304 (physically and electrically). See figs. 3-5 of Oikawa.

Regarding claim 14, Oikawa/Lai discloses the integrated circuit further comprising a second solid state amorphization region disposed beneath the D-mode gate contact at least within the first layer. See the rejection of claim 7.

Regarding claim 15, Oikawa/Lai discloses the integrated circuit wherein the D-mode and E-mode source and drain contacts 317/320 are coupled to the first layer 309, and the D-mode and E-mode gate contacts 315/316 are coupled to the barrier layer 304 (physically and electrically to control current flowing in the channel layer 303). See figs. 3-5 of Oikawa.

Regarding claims 16, 17, Oikawa/Lai discloses the integrated circuit comprising all claimed limitations. See col. 2, line 62 col. 4, line 59 of Oikawa, and col. 3, lines 18-27 of Lai.

Regarding claim 29, Oikawa discloses the integrated circuit comprising all claimed limitations as discussed in claim 28, except for expressly teaching a solid state amorphization region beneath the E-mode gate contact at least within the single barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the E-mode gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Oikawa to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 30, Oikawa/Lai discloses the integrated circuit wherein the solid state amorphization region includes at least one compound including at least one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 31, Oikawa/Lai discloses the integrated circuit wherein the solid state amorphization region includes a plurality of compounds, wherein at least one of the compounds includes one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium, and at least one of the compounds includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

]

Regarding claim 32, Oikawa/Lai discloses the integrated circuit wherein the multi-layer structure further comprises at least an epitaxial second layer 307 between the barrier layer 304 and the first layer 309. See figs. 3-5 of Oikawa.

Regarding claim 33, Oikawa/Lai discloses the integrated circuit wherein the barrier layer 304 is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the solid state amorphization region is within the implant region. See col. 2, line 62 col. 4, line 59 of Oikawa, and col. 3, lines 18-27 of Lai.

9. Claim(s) 7 and 12 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Imoto et al. (US 6,166,404), in view of U.S. Patent No. 6,452,221 to Lai et al.

Regarding claim 7, Imoto discloses an integrated circuit, as shown in fig. 1, comprising:

a depletion mode (D-mode) field effect transistor (DFET) and an enhancement mode (E-mode) EFET in a multi-layer structure 51&61,

wherein the multi-layer structure 51&61 includes a semiconductor substrate 51 overlaid with a plurality of epitaxial semiconductor layers 61 common to the DFET and EFET, including a channel layer 53 overlaid by a single barrier layer 56 overlaid by a single etch stop layer 57 overlaid by a first layer 58 overlaid by a second layer 84 adjacent to the first layer 58,

wherein the E-mode and D-mode FETs each include source/drain contacts 281A/B, 282A/B, and a gate contact 271/272, respectively,

wherein the source and drain contacts of the D-mode FET and the E-mode FET are coupled to, or in contact with, the second layer 84;

wherein the gate contact 272 of the D-mode FET is coupled to, or in contact with, the first layer 58, and

wherein the gate contact 271 of the E-mode FET is coupled to, or in contact with, the single barrier layer 56.

Imoto does not teach a solid state amorphization region beneath the D-mode gate contact within the first layer and a solid state amorphization region beneath the E-mode gate contact within single the barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Imoto to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 12, Imoto discloses an integrated circuit, as shown in fig. 1, comprising:

a depletion mode (D-mode) field effect transistor (DFET) and an enhancement mode (E-mode) EFET in a multi-layer structure 51&61,

wherein the multi-layer structure includes a semiconductor substrate 51 overlaid with a plurality of epitaxial semiconductor layers 61 common to the D-mode and E-mode FETs, including a channel layer 53 overlaid by a single barrier layer 56 overlaid by a single etch stop layer 57 overlaid by at least by a first layer 58;

wherein the D-mode and E-mode FETs each include source/drain contacts 281A/B, 282A/B and a gate contact 271/272,

wherein the source and drain contacts of the D-mode FET and the E-mode FET are coupled to, or in contact with, the first layer overlying the channel layer 53,

wherein a gate contact 272 of the D-mode FET is coupled to one of the first layer 58 and the single barrier layer 304 (the gate contact 316 is physically coupled to, or in contact with, the first layer 58),

wherein a gate contact 271 of the E-mode FET is physically coupled to, or in contact with, the first layer 58.

Imoto does not expressly teach about a solid state amorphization region beneath the E-mode gate contact at least within the single barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the E-mode gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Imoto to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the

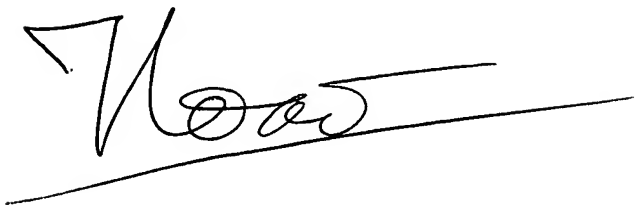
adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Conclusion

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke, can be reached on (571)272-1657. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.



Dao H. Nguyen
Art Unit 2818
November 12, 2007